AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A method of forming a polysilicon thin film transistor, comprising:

depositing an amorphous silicon layer over a substrate;

crystallizing the amorphous silicon layer into a polycrystalline silicon layer;

patterning the polycrystalline silicon layer to form a polysilicon active layer for a thin film transistor;

depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition;

applying heat to anneal the gate insulation layer under the vacuum condition, wherein there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer and wherein the applying heat to anneal the gate insulation layer is conducted under [[an]] atmosphere including at least H_2; and

forming a gate electrode on the annealed gate insulation layer.

Claim 2 (Cancelled).

Claim 3 (Original): The method of claim 1, wherein applying the heat to anneal the gate insulation layer is performed at a temperature ranging from 400 to 600 degrees Celsius.

Claim 4 (Currently Amended): The method of claim 1, wherein the vacuum condition for applying the heat to anneal[[annealing]] the gate insulation layer is a pressure ranging from 50 to 5000 mTorr.

Claim 5 (Previously Presented): The method of claim 1, wherein depositing silicon oxide includes using a plasma enhanced chemical vapor deposition (PECVD) method.

Claim 6 (Original): The method of claim 1, wherein crystallizing the amorphous silicon layer includes applying heat to the amorphous silicon layer using an excimer laser.

Claim 7 (Currently Amended): The method of claim 1, wherein applying heat occurs in [[the]] atmosphere of a vacuum chamber that also includes at least one of N_2, O_2, N_2O and NO.

Claim 8 (Currently Amended): A[[The]] method of [[claim 1,]]forming a polysilicon thin film transistor, comprising:

depositing an amorphous silicon layer over a substrate;

crystallizing the amorphous silicon layer into a polycrystalline silicon layer;

patterning the polycrystalline silicon layer to form a polysilicon active layer for a thin film transistor;

depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition;

applying heat to anneal the gate insulation layer under the vacuum condition; and

forming a gate electrode on the annealed gate insulation layer, wherein the difference of flat band voltage (ΔV_{fb}) between initial flat band voltage [V_{fb}(initial)] and flat band voltage after Fowler-Nordheim stress [V_{fb}(FNS)] is less than 0.5 V after applying the heat to anneal the gate insulation layer.

Claim 9 (Original): The method of claim 1, wherein the temperature of annealing the gate insulation layer is higher than the temperature of depositing the silicon oxide.

Claim 10 (Cancelled).

Claim 11 (Currently Amended): A method of forming a polysilicon thin film transistor, comprising:

forming a buffer layer over a substrate;

depositing an amorphous silicon layer over the buffer layer;

crystallizing the amorphous silicon layer into a polycrystalline silicon layer;

patterning the polycrystalline silicon layer to form a polysilicon active layer;

depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition;

applying heat to anneal the gate insulation layer under the vacuum condition, wherein there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer and wherein the applying heat to anneal the gate insulation layer is conducted under [[an]] atmosphere including at least H_2;

forming a gate electrode on the annealed gate insulation layer;

applying dopants to the polysilicon active layer to form source and drain regions;

forming an interlayer insulator to cover the gate electrode, the gate insulation layer and the source and drain regions;

forming source and drain contact holes in the interlayer insulator to expose portions of the source region and the drain region, respectively; and

forming source and drain electrodes.

Claim 12 (Cancelled).

Claim 13 (Original): The method of claim 11, wherein applying the heat to anneal the gate insulation layer is performed at a temperature ranging from 400 to 600 degrees Celsius.

Claim 14 (Currently Amended): The method of claim 11, wherein the vacuum condition for applying the heat to anneal[[annealing]] the gate insulation layer is a pressure ranging from 50 to 5000 mTorr.

Claim 15 (Currently Amended): The method of claim 11, wherein the gate insulation layer is formed by ~~depositing silicon oxide includes~~ using a plasma enhanced chemical vapor deposition (PECVD) [[(PEVCD)]] method.

Claim 16 (Original): The method of claim 11, wherein crystallizing the amorphous silicon layer includes applying heat to the amorphous silicon layer using an excimer laser.

Claim 17 (Original): The method of claim 11, wherein the buffer layer includes at least one of silicon oxide ($Si0_x$) and silicon nitride (SiN_x).

Claim 18 (Original): The method of claim 11, wherein applying dopants includes applying p-type ions.

Claim 19 (Original): The method of claim 18, wherein the p-type ions are boron ions.

Claim 20 (Original): The method of claim 11, wherein applying dopants includes applying n-type ions.

Claim 21 (Original): The method of claim 20, wherein the n-type ions are phosphorous ions.

Claim 22 (Currently Amended): The method of claim 11, wherein applying heat occurs in [[the]] atmosphere of a vacuum chamber that also includes ~~including~~ at least one of N_2, [[H_2,]] O_2, N_2O and NO.

Claim 23 (Currently Amended): A[[The]] method of [[claim 11,]]forming a polysilicon thin film transistor, comprising:

forming a buffer layer over a substrate;

depositing an amorphous silicon layer over the buffer layer;

crystallizing the amorphous silicon layer into a polycrystalline silicon layer;

patterning the polycrystalline silicon layer to form a polysilicon active layer;

depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition;

applying heat to anneal the gate insulation layer under the vacuum condition;

forming a gate electrode on the annealed gate insulation layer;

applying dopants to the polysilicon active layer to form source and drain regions;

forming an interlayer insulator to cover the gate electrode, the gate insulation layer and the source and drain regions;

forming source and drain contact holes in the interlayer insulator to expose portions of the source region and the drain region, respectively; and

forming source and drain electrodes, wherein the difference of flat band voltage (ΔV_{fb}) between initial flat band voltage [V_{fb}(initial)] and flat band voltage after Fowler-Nordheim stress [V_{fb}(FNS)] is less than 0.5 V after applying the heat to anneal the gate insulation layer.

Claim 24 (Original): The method of claim 11, wherein the temperature of annealing the gate insulation layer is higher than the temperature of depositing the silicon oxide.

Claim 25 (Cancelled).

Claim 26 (Previously Presented): A method of forming a polysilicon thin film transistor, comprising:

depositing an amorphous silicon layer over a substrate;

crystallizing the amorphous silicon layer into a polycrystalline silicon layer;

patterning the polycrystalline silicon layer to form a polysilicon active layer for a thin film transistor;

depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition;

applying heat to anneal the gate insulation layer under a vacuum condition; and

forming a gate electrode on the annealed gate insulation layer,

wherein the difference of flat band voltage (ΔV_{fb}) between initial flat band voltage [V_{fb}(initial)] and flat band voltage after Fowler-Nordheim stress [V_{fb}(FNS)] is less than 0.5 V after applying the heat to anneal the gate insulation layer.